REMARKS/ARGUMENTS

This Amendment is filed in response to the non-final Office Action mailed August 25, 2005. Claims 1, 3-9, 11-13 and 15-20 have been rejected. Claims 1, 3, 4, 6, 8, 9, 11, 13, 19 and 20 have been amended. Claims 1, 3-9, 11-13, and 15-20 are pending after entry of the present Amendment. It is respectfully submitted that the pending claims define allowable subject matter. Applicants respectfully request reconsideration of the application in view of the above amendments and the following remarks submitted in support thereof.

Discussion of Rejection of Claims 1, 3-9, 11-13 and 15-20 under 35 U.S.C. § 112

First Paragraph

In Sections 3 and 4 of the Office Action, the Examiner rejected Claims 1, 3-9, 11-13 and 15-20 under 35 U.S.C. § 112, first paragraph, because a new limitation "a different rule of instruction scheduling" is not found or enabled in the originally filed disclosure.

Examiner's rejection is respectfully traversed. Applicants have amended Claims 1, 8, 19 and 20 to remove any references to "a different rule of instruction scheduling." In view of the foregoing, Applicants respectfully submit that the claims overcome the Examiner's rejection under 35 U.S.C. § 112.

Discussion of Rejection of Claims 1-6 and 8-20 under 35 U.S.C. § 102(b)

In Section 11 of the Office Action, the Examiner rejected Claims 1-6 and 8-20 under 35 U.S.C. § 102(b) as being anticipated by Aho et al., "Compilers: Principles, Techniques, and Tools."

The Examiner's rejection is respectfully traversed. Applicants respectfully note that Claims 2, 10 and 14 were canceled by Applicants in a prior Amendment. Applicants have amended independent Claims 1, 8, 19 and 20 to further clarify that a hypothetical machine model is generated that is based on a rule of instruction scheduling for each of at least two target machines so that a resulting rule of instruction scheduling of the hypothetical machine model is more restrictive than either of the respective rules of instruction scheduling for each of the two target machines, and that the hypothetical machine module is capable of operating satisfactorily on either of the two target machines. Applicants have re-read Aho et al. and Applicants respectfully submit that nothing in Aho et al. teaches the generation of a hypothetical machine model that incorporates the characteristics (by way of rules of instruction scheduling) of at least two target machines of interest so that the hypothetical machine model can operate satisfactorily on either of the two target machines.

Rather, Aho et al. first discloses that the phases in which a compiler operates are collected into a front end and a back end, the front end primarily dependent on a source program and "largely independent of a target machine," and the back end including those portions of the compiler that depend on the target machine. S*ee* Section 1.5, page 20. Aho et al. then discloses taking the front end of a compiler and redoing its associated back end "to produce a compiler for the same source program on *a different machine*." *See* Section 1.5, page 20. It necessarily follows therefore, based on the teachings of Aho et al., that each time the back end is modified a new compiler for *a different machine* results and any binary (target program) produced by that new compiler will uniquely correspond *to the different machine*. In other words, where there are two different machines (two target machines) you will also have two different binaries (target programs) produced for the same source code on those machines, one uniquely optimized to run on one target machine and the other uniquely

optimized to run on a different target machine. *See* Sections 1.3 and 1.5. Conversely, the claims of the present invention teach a method of simultaneous code optimization for at least two different target machines by generating *a* hypothetical machine module that is capable of operating on each of at least two target machines, as recited in the claims of the present application. By utilizing the hypothecial machine module, the desired outcome of embodiments of the present Application is to obtain *one given binary* that is optimized to run on *each* target machine (*see* present Application, page 12, lines 1-5).

The foregoing demonstrates that Aho et al. does not teach each and every element and limitation of amended Claims 1, 8, 13 and 19. Consequently, Aho et al. does not anticipate dependent Claims 1, 8, 13 and 19 and Applicants respectfully request that the 102 rejection be withdrawn.

Claims 3-6, 9, 11, 12 and 15-18 indirectly or directly depend for independent Claims 1, 8, 13 and 19 respectively and, as these dependent claims depend from allowable base claims, they too are not anticipated by Aho et al. Applicants respectfully request, therefore, that the rejection of these dependent claims also be withdrawn.

Discussion of Rejection of Claim 7 under 35 U.S.C. §103(a)

In Section 8 of the Office Action, the Examiner rejected Claim 7 under 35 U.S.C. §103(a) as being unpatentable over Aho et al. in view of "UltraSPARC-III: Designing Third-Generation 64-Bit Performance" (hereinafter III) and Sun Microsystems press release of May 1998 (hereinafter II).

The Examiner's rejection is respectfully traversed. Assuming, *arguendo*, that there is a suggestion or motivation to combine the cited references, a proposition with which the

Applicants would disagree, the combination still fails to teach each and every element and limitation of independent Claim 1, as discussed above, from which Claim 7 depends.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. § 103(a) rejection for pending Claim 7.

Discussion of Examiner's Response to Arguments

In Section 9 of the Office Action, the Examiner responded to Applicants remarks submitted in the amendment filed by Applicants on May 27, 2005. In the response, the Examiner states that Applicants' argument that Aho et al. fails to provide any disclosure of targeting at least two target machines is found unpersuasive. Applicants have considered the Examiner's response and the citations provided in support of the response and respectfully note that Applicants argument with respect to Aho et al. is not whether two machines can be targeted but rather how the two machines are targeted. As previously discussed, Aho et al. discloses modifying the back end of a compiler to produce a compiler for the same source program on a different machine, the result of which is the compilation of the same source program on respective compilers to produce a binary optimized for a first target machine and a different binary optimized for a different second target machine. Applicants again respectfully note that an objective of the present Application is to obtain *a given binary* (not multiple binaries) that is optimized to run on *each* target machine. This objective is accomplished, as recited in the claims of the present Application, by generating a hypothetical machine module that is capable of operating on *each* of at least two target machines.

Conclusion

In view of the foregoing, the Applicant respectfully submits that all the pending Claims 1, 3-9, 11-13 and 15-20 are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present amendment, the Examiner is requested to contact the undersigned at (408) 749-6920. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP303). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, L.L.P.

Gina A. Bibby
Reg. No. 57,407

Martine Penilla & Gencarella, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
Telephone: (408) 774-6920
Customer Number 32291